MAEDA et al.
Serial No. 10/714,935
Response to Office Action dated July 7, 2006

REMARKS

Reconsideration and allowance of the subject patent application are respectfully requested.

Amendments of a formal nature have been made to the specification and abstract.

Claims 1-3, 5 and 7-9 were rejected under 35 U.S.C. Section 102(b) as allegedly being "anticipated" by Fujitani (JP 2-312099).

The office action alleges that the circuit including the three NAND gates G in Figure 1 of Fujitani corresponds to the "different circuit" of claims 1, 8 and 9. While not agreeing with or acquiescing in this characterization, claims 1, 8 and 9 have been amended to require that the different circuit be one "which is different from the unit circuits and not involved in operation of the shift register so that an output of the circuit is not supplied to the unit circuits". Non-limiting example support for this feature can be found, for example, on page 11, lines 20-22 of the specification and throughout the Figures (e.g., Figure 1, 10, 11, 12 and 13).

The NAND gates of Fujitani are directly involved in the operation of the shift register and, according to the Fujitani arrangement, are required to be provided between the output stage of a flip-flop and the input stage of a directly subsequent flip-flop. The NAND gates thus are part of the shift register. Consequently, Fujitani does not disclose the "different circuit" of claims 1, 8 and 9 and, for at least this reason, Fujitani cannot anticipate the claims.

Claims 3, 5 and 7 depend from claim 1 and are not anticipated by Fujitani because of this dependency and because of the additional patentable features recited therein.

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Claims 13 and 14 were rejected under 35 U.S.C. Section 102(b) as allegedly being "anticipated" by Washio et al. (JP 2001-135093). The office action alleges that the inverter 24 shown in Figure 1 of Washio corresponds to the "different circuit" of claim 13. While not agreeing with or acquiescing in this characterization, claim 13 has been amended along the lines of claims 1, 8 and 9 and requires that the "different circuit" be one "which is different from the unit circuits and not involved in operation of the shift register so that an output of the circuit is not supplied to the unit circuits". The inverter 24 of Washio et al. receives a clock signal supplied to the corresponding stage, when the switching means is closed. The output of inverter 24 is supplied to the flip-flop two stages behind as a reset signal. Thus, inverter 24 is directly involved in the shift register operation and is part of the shift register. Consequently, Washio et al. does not disclose the "different circuit" of claim 13 and, for at least this reason, Washio et al. cannot anticipate this claim or its dependent claim 14.

Claims 4, 6 and 10 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over Fujitani in view of Karube et al. (U.S. Patent No. 6,072,456). Karube et al. does not remedy the deficiencies of Fujitani with respect to claims 1 and 9, from which claims 4, 6 and 10 depend. Moreover, Karube et al. is deficient with respect to the features of these dependent claims.

For example, with respect to claims 4 and 6, the office action references Figure 2 of Karube et al. as showing "a circuit for shift register having separate shift registers disposed between other shift registers ..." Figure 2 of Karube et al. shows shift registers 101, 102, 103 and 104 each respectively associated with a corresponding signal line group. See also Karube et al., col. 4, lines 9 et seq. However, Karube et al. does not show

successive unit circuits for one shift register of a first system being arranged between successive unit circuits for another shift register of a second different system.

Claims 11 and 12 stand rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over Fujitani. However, even assuming that the use of analog or digital data in Fujitani could be shown to have been obvious and that the circuits of Fujitani can be viewed as including one of the circuits mentioned in claims 11 and 12, respectively, Fujitani is still deficient with respect to claim 9, from which claims 11 and 12 depend.

Claims 15 and 16 under 35 U.S.C. Section 103(a) as allegedly being "obvious" over Washio et al. in view of Brownlow et al. (U.S. Patent No. 6,232,946). Brownlow is alleged to teach "the use of polysilicon transistors for fabricating driver (sic) monolithically on a display substrate." Brownlow et al. does not remedy the deficiencies of Washio with respect to claim 13, from which claims 15 and 16 depend. Consequently, claims 15 and 16 patentably distinguish from the proposed combination for at least this reason.

New claims 17-20 have been added. Non-limiting example support for the subject matter of these claims can be found, for example, in Figures 1 and 11 and their accompanying descriptions. The applied references do not show, among other things, circuits different from unit circuits disposed in the physical spaces between adjacent unit circuits, wherein outputs from the respective different circuits are not supplied to any of the unit circuits. Consequently, claim 17 and its dependent claims are believed to patentably distinguish from these references.

The pending claims are believed to be allowable and favorable office action is respectfully requested. Should the Examiner feel that an interview

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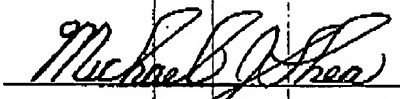
with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,
NIXON & VANDERHYE P.C.

By: 
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